

FEATURES

- 2 A Load Current**
- 45 mΩ On Resistance**
- User-Settable Current Limit**
- 12 μA Typical Quiescent Current**
- 10 nA Typical Shutdown Current**
- 40 nA Typical Switch Off Leakage**
- Short-Circuit Protection**
- Thermal Shutdown**
- FAULT Output**
- Small, 16-Lead QSOP Package**

APPLICATIONS

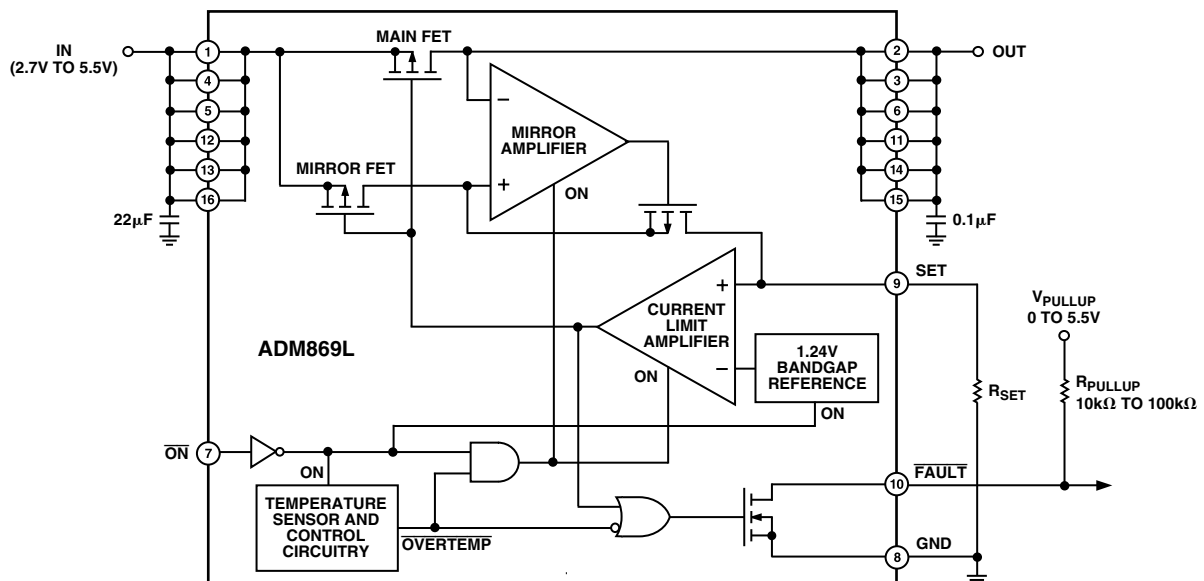
- Desktop Computers**
- Palmtop Computers**
- Notebook Computers**
- Hand-Held Instruments**
- Universal Serial Bus (USB)**

GENERAL DESCRIPTION

The ADM869L is a logic controlled P-channel switch with low on resistance, capable of sourcing up to 2 A from supply voltages between 2.7 V and 5.5 V. A user-settable current limit allows the trip current to be set between 400 mA and 2 A with an accuracy of $\pm 21\%$. This allows the system power supply to be protected against short circuits and surge currents in peripheral loads powered via the ADM869L. Over-current and over-temperature conditions are signalled by a $\overline{\text{FAULT}}$ output.

The ADM869L also offers low quiescent current of typically 12 μA and shutdown current of typically 10 nA.

FUNCTIONAL BLOCK DIAGRAM



REV. B

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ADM869L—SPECIFICATIONS ($V_{CC} = 3.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ ¹, unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-------|-------|---------|------------------|---|
| Operating Voltage Range | 2.7 | | 5.5 | V | |
| Quiescent Current | | 12 | 20 | μA | $V_{IN} = 5\text{ V}$, $\overline{\text{ON}} = \text{GND}$, $I_{OUT} = 0\text{ A}$, 0°C to 85°C |
| | | 12 | 25 | μA | $V_{IN} = 5\text{ V}$, $\overline{\text{ON}} = \text{GND}$, $I_{OUT} = 0\text{ A}$, -40°C to $+85^\circ\text{C}$ |
| Shutdown Supply Current | | 0.01 | 2 | μA | $\overline{\text{ON}} = V_{IN} = V_{OUT} = 5.5\text{ V}$ |
| Off-Switch Current | | 0.04 | 2 | μA | $\overline{\text{ON}} = V_{IN} = V_{CC}$, $V_{OUT} = 0\text{ V}$ |
| Undervoltage Lockout | 2.0 | 2.3 | 2.6 | V | Rising Edge, 1% Hysteresis |
| On Resistance | | 38 | 70 | $\text{m}\Omega$ | $V_{IN} = 4.75\text{ V}$ |
| | | 45 | 90 | $\text{m}\Omega$ | $V_{IN} = 3.0\text{ V}$ |
| Nominal Current-Limit Setting Range | 0.4 | | 2.4 | A | $R_{SET} = 1\%$ Tolerance ² |
| Current-Limit Amplifier Threshold | 1.178 | 1.240 | 1.302 | V | V_{SET} Required to Turn Off Switch ³ |
| I_{OUT}/I_{SET} Current Ratio | 810 | 955 | 1100 | A/A | $I_{OUT} = 1\text{ A}$, $V_{OUT} > 1.6\text{ V}$ |
| $\overline{\text{ON}}$ Input Low Voltage, V_{IL} | | | 0.8 | V | $V_{IN} = 2.7\text{ V}$ to 5.5 V |
| $\overline{\text{ON}}$ Input High Voltage, V_{IH} | 2.0 | | | V | $V_{IN} = 2.7\text{ V}$ to 3.6 V |
| | 2.4 | | | V | $V_{IN} = 4.5\text{ V}$ to 5.5 V |
| ON Input Leakage | | 0.01 | ± 1 | μA | $V_{\overline{\text{ON}}} = 5.5\text{ V}$ |
| Current-Limit Amplifier Input Bias Current | | 0.05 | ± 3 | μA | $V_{SET} = 1.24\text{ V}$, $I_{OUT} = 0\text{ A}$ |
| $\overline{\text{FAULT}}$ Logic Output Low Voltage | | | 0.4 | V | $I_{SINK} = 1\text{ mA}$, $V_{SET} = 1.4\text{ V}$ |
| $\overline{\text{FAULT}}$ Output High Leakage Current | | 0.05 | 1 | μA | $V_{FAULT} = 5.5\text{ V}$, $V_{SET} = 1\text{ V}$ |
| Slow Current-Loop Response Time | | 10 | | μs | 20% Current Overdrive, $V_{IN} = 5\text{ V}$ |
| Fast Current-Loop Response Time | | 4 | | μs | |
| Turn-On Time | | 100 | 300 | μs | $V_{IN} = 5\text{ V}$, $I_{OUT} = 500\text{ mA}$ |
| | | 200 | | μs | $V_{IN} = 3\text{ V}$, $I_{OUT} = 500\text{ mA}$ |
| Turn-Off Time | 1 | 2 | 30 | μs | $V_{IN} = 5\text{ V}$, $I_{OUT} = 500\text{ mA}$ |

NOTES

¹Specifications to -40°C are guaranteed by design, not tested.

²Guaranteed by design. Derived from the I_{SET} current ratio, current-limit amplifier and external set resistor accuracies.

³Tested with $I_{OUT} = 200\text{ mA}$ and V_{SET} adjusted until $(V_{IN} - V_{OUT}) \geq 0.8\text{ V}$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

| | | |
|--|-------|-------------------------------------|
| IN to GND | | -0.3 V to +6 V |
| ON, FAULT to GND | | -0.3 V to +6 V |
| SET, OUT to GND | | -0.3 V to (V _{IN} + 0.3 V) |
| Maximum Continuous Switch Current | | 3 A |
| Continuous Power Dissipation (T _A = 70°C) | | 667 mW |
| QSOP (Derate 8.3 mW/°C above 70°C) | | |
| Operating Temperature Range | | |
| Industrial (A Version) | | -40°C to +85°C |
| Storage Temperature Range | | -65°C to +150°C |
| Lead Temperature (Soldering, 10 sec) | | 300°C |
| ESD Rating (Outputs) | | 15 kV |
| (Other Pins) | | 2 kV |

*This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

THERMAL CHARACTERISTICS

16-Lead QSOP Package:

θ_{JA} = 50°C/W, θ_{JC} = 10°C/W

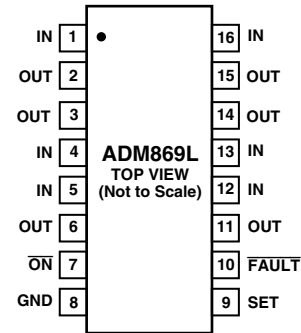
ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|------------|-------------------|---------------------|----------------|
| ADM869LARQ | -40°C to +85°C | 16-Lead QSOP | RQ-16 |

PIN FUNCTION DESCRIPTIONS

| Pin | Mnemonic | Function |
|---------------------|----------|--|
| 1, 4, 5, 12, 13, 16 | IN | Input to P-Channel MOSFET Source and Supply to Chip Circuitry. Bypass IN with a 22 μF capacitor to ground. |
| 2, 3, 6, 11, 14, 15 | OUT | Output from P-Channel MOSFET Drain. Bypass OUT with a 0.1 μF capacitor to ground. |
| 7 | ON | Digital Input. Active-low switch enable (logic 0 turns the switch on). |
| 8 | GND | Ground. |
| 9 | SET | Current Limit Setting Input. A resistor from set to ground sets the current limit. Refer to Current Limit section. |
| 10 | FAULT | Open-Drain Digital Output. FAULT goes low when the current limit is exceeded or the die temperature exceeds 135°C. During startup, FAULT remains low for the turn-on time + 50 μs. |

PIN CONFIGURATION

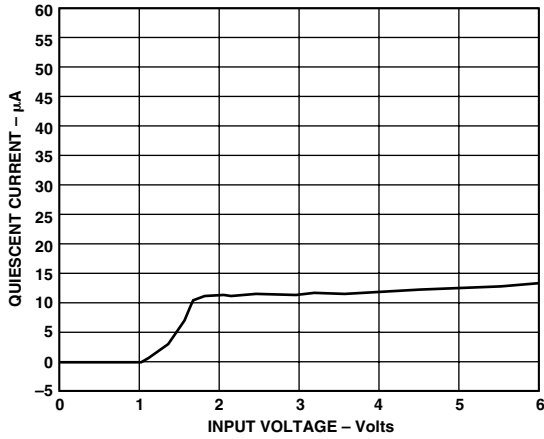


CAUTION

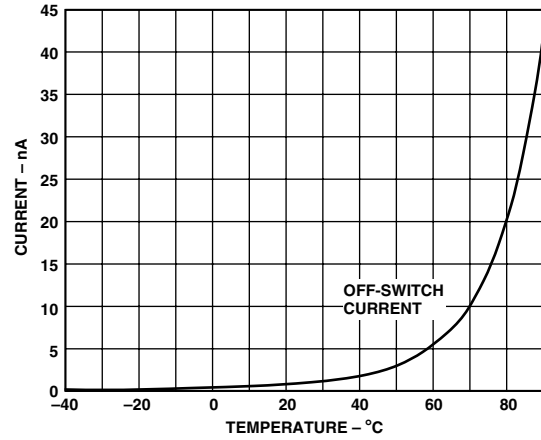
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM869L features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



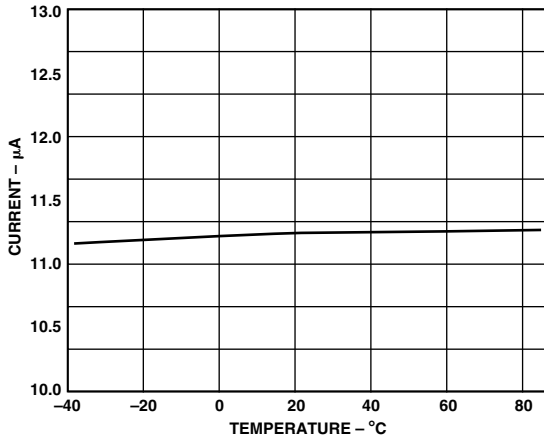
ADM869L—Typical Performance Characteristics



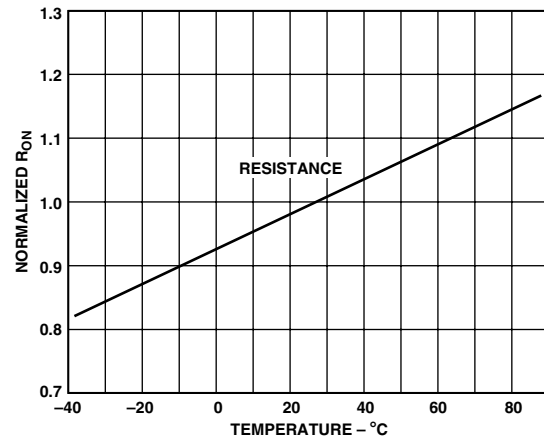
TPC 1. Quiescent Current vs. Input Voltage



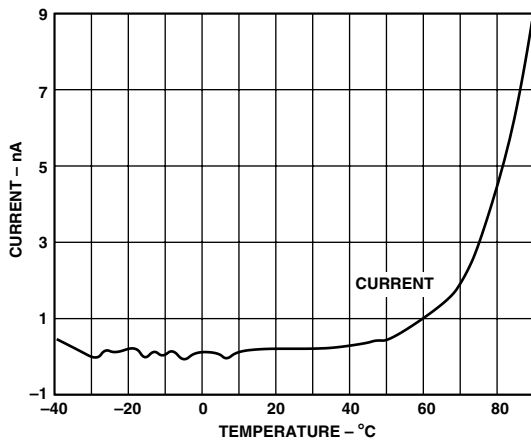
TPC 4. Off-Switch Current vs. Temperature



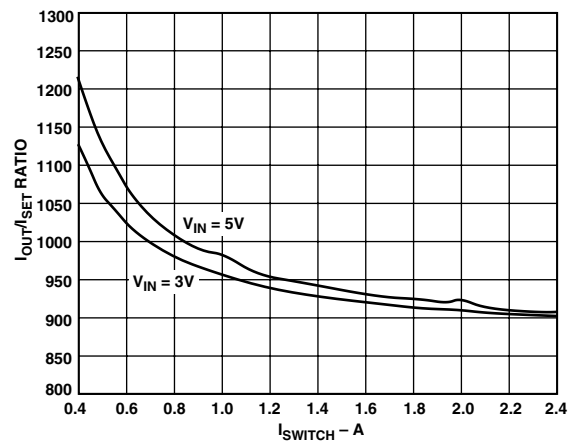
TPC 2. Quiescent Current vs. Temperature



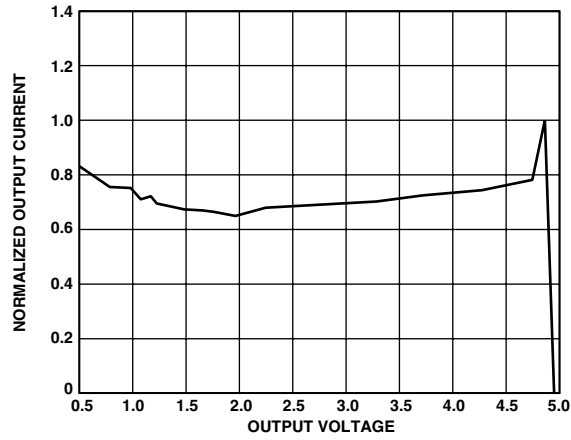
TPC 5. Normalized On Resistance vs. Temperature



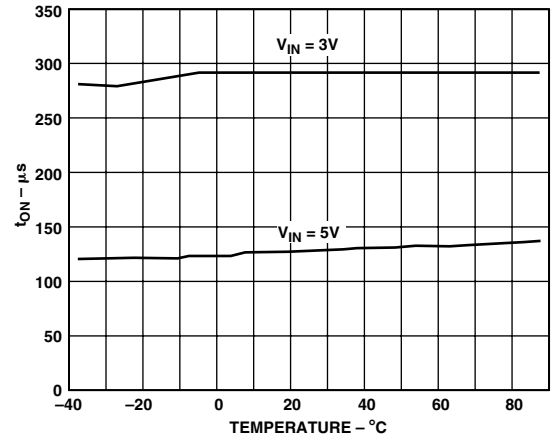
TPC 3. Off-Supply Current vs. Temperature



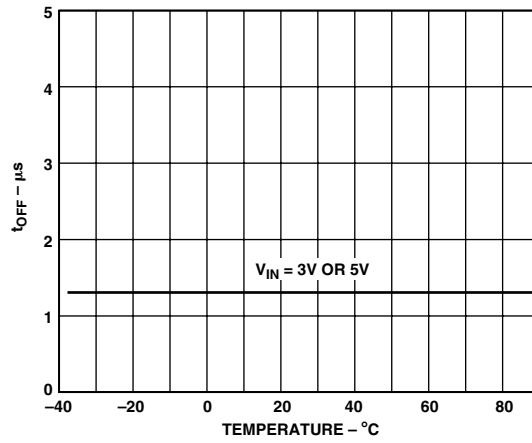
TPC 6. I_{OUT}/I_{SET} Ratio vs. Switch Current



TPC 7. Normalized Output Current vs. Output Voltage

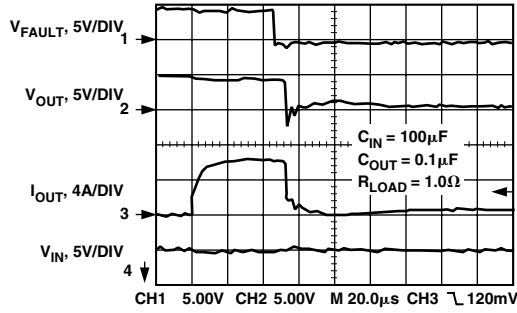


TPC 8. Turn-On Time vs. Temperature

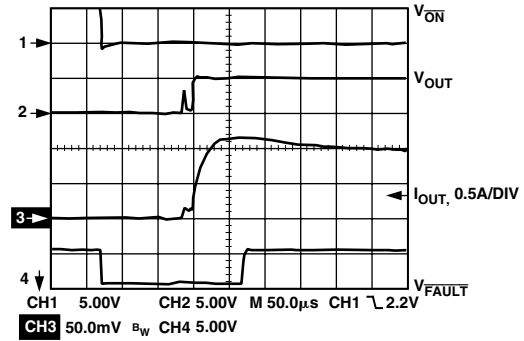


TPC 9. Turn-Off Time vs. Temperature

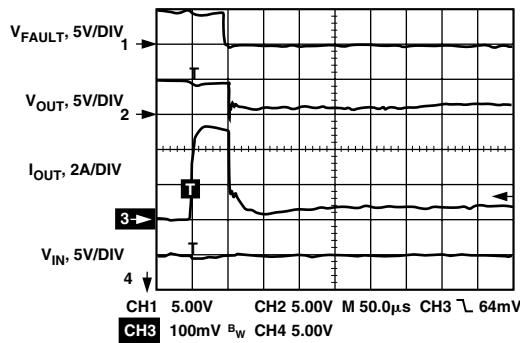
ADM869L



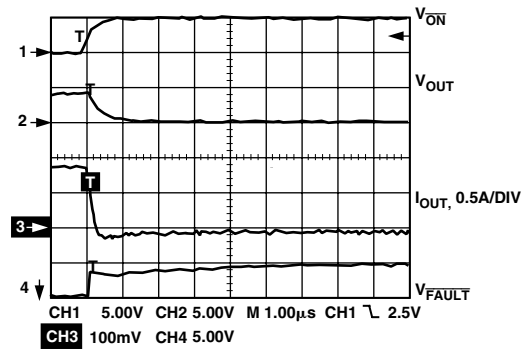
TPC 10. Fast Current-Limit Response



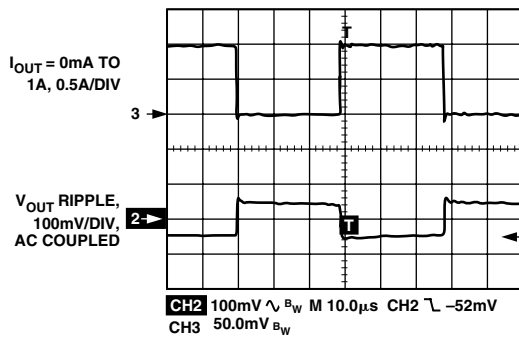
TPC 13. Switch Turn-On Time



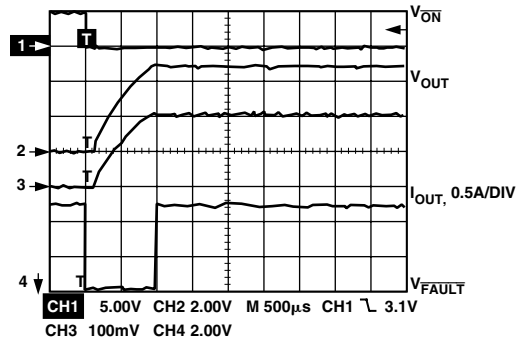
TPC 11. Slow Current-Limit Response



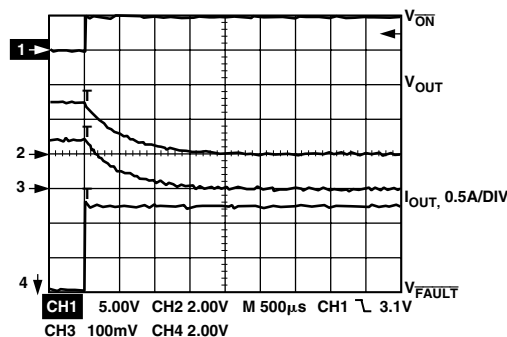
TPC 14. Switch Turn-Off Time



TPC 12. Load Transient Response



TPC 15. USB Circuit Output Rise Time



TPC 16. USB Circuit Output Fall Time

FUNCTIONAL DESCRIPTION

The ADM869L comprises a high-current P-channel switch controlled by an active-low logic input $\overline{\text{ON}}$ (Pin 7). When $\overline{\text{ON}}$ is low, the internal circuitry of the ADM869 is powered up and the output of the current-limit amplifier is low, providing gate drive to the switching FET. When $\overline{\text{ON}}$ is high, the internal circuitry is powered down and the current consumption is typically 100 nA.

It should be noted that the ADM869L is not a bidirectional switch, so V_{IN} must always be higher than V_{OUT} .

CURRENT LIMIT

When the switch is turned on, a smaller mirror switch passes a proportionate current equal to $I_{\text{OUT}}/955$. The mirror amplifier maintains this relationship by keeping the drain of the mirror FET at the same voltage as the main FET, and drives the mirror current through the current-limit resistor R_{SET} , which is connected between the noninverting input of the current limit amplifier and ground. An on-chip bandgap reference of 1.24 V is connected to the inverting input of the current-limit amplifier. When the load current exceeds the preset limit, the voltage across R_{SET} exceeds 1.24 V, and the output voltage of the current-limit amplifier rises, reducing the gate drive to the FETs.

If, for example, a 1 A current limit is required, $R_{\text{SET}} = 1.24 \text{ V} / 1.047 \text{ mA} = 1.184 \text{ k}\Omega$. Note that $I_{\text{OUT}}/I_{\text{SET}}$ varies depending on current so please refer to TPC 6.

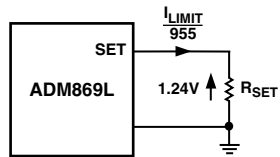


Figure 1. Setting the Current Limit

THERMAL SHUTDOWN

The thermal shutdown operates when the die temperature exceeds 135°C, turning off the switch. The thermal shutdown circuit has built-in hysteresis of 10°C, so the switch will not turn on again until the die temperature falls to 125°C. If the fault condition is not removed, the switch will pulse on and off as the temperature cycles between these limits.

FAULT OUTPUT

If either the current limit or the thermal shutdown is activated, $\overline{\text{FAULT}}$ will pull low. This is an open-drain output and requires a pull-up resistor of between 10 kΩ and 100 kΩ. Several $\overline{\text{FAULT}}$ outputs may be wire-OR'd to form a common interrupt line, as shown in Figure 2 or $\overline{\text{FAULT}}$ may be wire-OR'd to an existing interrupt line that has a resistive pull-up.

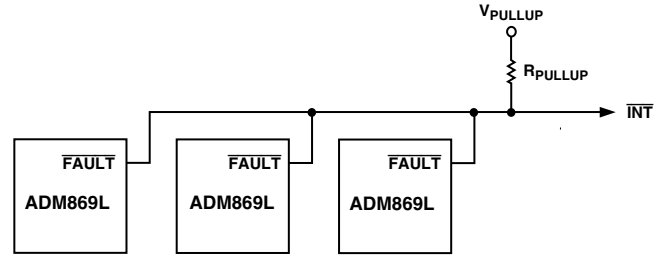


Figure 2. Wire Or'ing $\overline{\text{FAULT}}$ Outputs

During startup, the $\overline{\text{FAULT}}$ output goes low for the turn-on time plus 50 μs.

APPLICATIONS INFORMATION

INPUT FILTERING

To prevent the input voltage being pulled below the minimum operating voltage under transient short-circuit conditions, before the current limit has had time to operate, a reservoir capacitor should be connected from IN to GND. This does not need to be large, but should have a low ESR. A 22 μF ceramic type is suitable. Larger values will reduce the voltage drop still further.

OUTPUT CAPACITANCE

A 0.1 μF capacitor should be connected between OUT and GND to prevent the back e.m.f. of parasitic inductance from pulling OUT below ground during turn-off. For Universal Serial Bus (USB) applications, C_{OUT} should be at least 120 μF. This causes the output rise and fall times to be longer, as shown in the typical operating characteristics, but does not affect the turn-off time of the ADM869L itself.

LAYOUT CONSIDERATIONS

Printed circuit board tracks to and from the ADM869L should be as thick and as short as possible to minimize parasitic inductance and take full advantage of the fast response time of the switch. It is recommended that all input lines be connected together, close to the device. This ensures equal current distribution in all legs. If this is not possible, then all traces should be of equal width and length. The same rules apply for all output lines. Input and output capacitors should be placed as close to the device as possible (less than 5 mm).

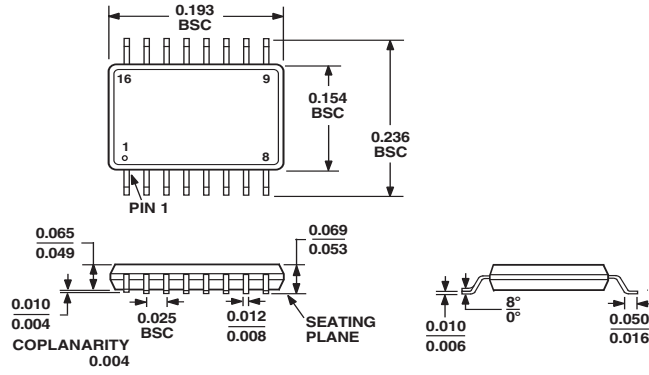
THERMAL CONSIDERATIONS

Under normal operating conditions, the worst-case power dissipation will be 518 mW with the highest specified on resistance and 3 V supply ($W = 2.4 \text{ A} \times 0.9 \text{ V}$). The package is capable of handling and dissipating this power, but heat dissipation can further be improved by providing a large area of copper in contact with the device pins, particularly IN and OUT.

OUTLINE DIMENSIONS

16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)

Dimensions shown in inches



COMPLIANT TO JEDEC STANDARDS MO-137AB

C01037-0-4/03(B)

Revision History

| Location | Page |
|--|------|
| 4/03—Data Sheet changed from REV. A to REV. B. | |
| Added ESD Caution | 3 |
| Updated OUTLINE DIMENSIONS | 8 |